METHOD AND APPARATUS FOR ELIMINATION OF EXCESSIVE FIELD OXIDE RECESS FOR THIN Si SOI

Background

[0001] The present disclosure relates to semiconductor device processing, and more particularly, to a method and apparatus for elimination of excessive field oxide recess for Thin Si SOI.

Related Art

[0002] A problem in the art has been discovered to exist in connection with an excessive field oxide recess for thin silicon SOI. The excessive field oxide recess leads to MOAT formations or voids occurring around bitcells and other structures in SOI. The MOATs have been found to form as a result of HF penetration that etches an insulative fill material, such as HDP, from the sidewalls of Si (at an interface between the Si and trench isolation material), coupled with areas of weak oxide at the top of a BOX (bottom oxide), and at the top Si interface. Etching of the two weak oxide regions accelerates the removal of the isolation material from around a given structure, thereby causing recession to occur into the BOX, thus undesirably forming a MOAT or void.

[0003] In one example, a problem exists in the area of weak oxide found at the top of the BOX layer near the interface of a 200A thick liner. This area of weak oxide functions as a stress relief mechanism. When the stress relief mechanism is coupled with the recession of HDP at the sidewalls of the shallow trench isolation (STI) corner region, formation of MOATS occurs, leading to formation of poly stringers and depressed device yields.

[0004] Accordingly, there is a need for an improved method and apparatus for overcoming the problems in the art as discussed above.

SUMMARY

[0005] According to one embodiment, a method of making a semiconductor device includes providing a substrate having a semiconductor layer over a first insulating layer and forming a second insulating layer on the semiconductor layer having a thickness not greater than about 100 Angstroms. The method further includes forming an anti-reflective coating (ARC) on the second insulating layer, etching an opening through the ARC, the second insulating layer, and the semiconductor layer, and into the first insulating layer. Additionally, the method includes forming a third insulating layer along a sidewall of the opening, filling the opening with dielectric fill material, removing the ARC and the second insulating layer, forming a gate dielectric, forming a conductive layer on the gate dielectric, and patterning the conductive layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The present invention is illustrated by way of example and not limited by the accompanying figures, in which like references indicate similar elements, and in which:

[0007] Figure 1 is a top-down view of a portion of an SOI semiconductor device;

[0008] Figures 2-9 include cross-sectional views of the SOI semiconductor device of Figure 1 at various steps of manufacture;

[0009] Figure 10 is a top-down view of a portion of an SOI semiconductor device according to an embodiment of the present disclosure; and

[0010] Figures 11-18 include cross-sectional views of the SOI semiconductor device of Figure 10 at various steps of manufacture according to an embodiment of the present disclosure.

[0011] Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve the understanding of the embodiments of the present invention.

DETAILED DESCRIPTION

[0012] According to the present disclosure, the embodiments eliminate various mechanisms in the formation of MOAT defects. For example, the embodiments eliminate a first mechanism that starts the formation of MOAT defects. Secondly, the embodiments address a second area that enables the MOAT defect, corresponding to the weak oxide at the bottom of the liner/top BOX and bottom Si interface. Accordingly, by eliminating the first and second mechanisms, the recession of the HDP by one or more HF cleans does not lead to any voids or areas for POLY stringers. Moreover, leakage current is diminished and yields for devices are improved. In one embodiment, the problems in the art are overcome by a re-engineering of an SOI integration for Thin SOI. Such a method includes, for example, changes in thicknesses for a PAD-Ox, a liner oxide, and an HDP fill process.

[0013] The first mechanism of the MOAT defect was discovered at the interface of the oxide and nitride, which corresponded to an approximate 35Å undercut. The undercut was created by a pre-clean 35 Å HF that was used prior to the trench liner deposition. The Oxide thickness was on the order of 145 Å. The second mechanism was the area under the 200A liner at the top of the box/top of the bottom Si interface. There was significant overlap of the liner that prohibited a uniform fill at the bottom of the liner. Accordingly, the area included a void at the bottom, which became a stress relief point. Through subsequent processing, the void at the top is recessed below the Si, due to HF etching and merges with the void at the bottom, thus developing into a MOAT defect that extends into the BOX.

[0014] In one embodiment of the present disclosure, the areas that were found to cause the MOAT defects around bitcell devices were resolved by changing the Thin SOI integration as discussed herein. For example, a Pad Ox thickness was changed from 145 Å to 90 Å to eliminate an undercut at the Nitride/Si interface. The liner was changed from a non-uniform 200Å liner to a uniform 40Å liner. In addition, the pre-clean was reduced from 35Å HF to 0Å HF.

[0015] Figure 1 is a top-down view of a portion of an SOI semiconductor device 10, having areas susceptible to field recessions, referred to herein as "moats." The present disclosure is directed to thin SOI semiconductor devices, wherein thin SOI refers to the silicon layer of the SOI being scaled to less than 1100 angstroms. An active region of device 10 is generally designated by the reference numeral 12. An isolation region of device 10 is generally designated by the reference numeral 14. Semiconductor device 10 further includes

transistor word lines, generally designated by reference numerals 16 and 18. An interface between an active region 12 and an isolation region 14 is generally designated by reference numeral 20. While the following discussion is particular to a single interface, it is equally applicable to more than one such interface of the semiconductor device 10.

[0016] Figures 2-9 include cross-sectional views of the SOI semiconductor device of Figure 1 at various steps of manufacture. Referring now to Figure 2, two views are shown indicated by reference numerals 22 and 24 that represent cross-sectional views of an SOI semiconductor wafer that has been processed up through FEOL (front end of line) trench etch. The SOI semiconductor substrate includes a silicon substrate 26, insulator layer 28, and silicon layer 30.

[0017] In one embodiment, the SOI semiconductor substrate includes a thin SOI substrate wherein layer 30 has a thickness on the order of less than 1100 angstroms. Layers 32 and 34 represent pad oxide (pad-OX) and nitride, respectively. The pad-OX layer 32 includes a sacrificial oxide that protects the underlying silicon during processing of the active regions. Pad-OX layer 32 has a thickness on the order of less than approximately 100Å. Nitride layer 34 has a thickness that depends on the lithographic technique used to pattern the active region (i.e., the node wavelength g-line, i-line, DUV, 193nm, etc.). For example, the nitride layer 34 could include a thickness on the order of less than 1500Å.

[0018] At this point in the manufacturing process, cross-sectional views 22 and 24 are similar. Note that processing of the semiconductor wafer up through FEOL trench etch results in a slight over etch into bottom oxide layer 28, also referred to herein as BOX. The over etch is on the order of zero to 100Å. In addition, the FEOL trench etch creates a sidewall interface between the active region 12 and the isolation region 14, wherein the sidewall includes exposed area of silicon layer 30, pad-OX 32, and nitride layer 34. The sidewall will further include an exposed area of the BOX 28 resulting from the overetch, the exposed area having a depth approximately on the order of zero to 100Å. In addition, there could potentially be an undercut (or void) at the bottom of the trench in the region of the overetch, in particular, at the silicon and BOX interface.

[0019] Referring now to Figure 3, the two views indicated by reference numerals 22 and 24 are similar to those shown in Figure 2, wherein the SOI semiconductor device 10 has been further processed up to a pre-liner, post FEOL trench etch. Accordingly, views 22 and 24

have the following differences. A cleaning operation is performed to create an undercut 36 at the nitride/pad-OX interface, to ensure a complete coverage of the subsequently formed preliner 38. Semiconductor device 10 is then processed with an oxide to form the non-conformal preliner 38 on the sidewall interface between regions 12 and 14. Non-conformal preliner 38 has a thickness that varies between on the order of 100-250Å. Formation of the non-conformal preliner 38 also creates a void region 40, wherein the void region can include a vacancy, cavity, crevice, open region or the like. The void region 40 becomes significant during further processing that occurs post pre-liner.

[0020] Referring now to Figure 4, the two views indicated by reference numerals 22 and 24 are similar to those shown in Figure 3, wherein the SOI semiconductor device 10 has been further processed with a fill step, densification and CMP (chemical mechanical polish), up to post-CMP, post pre-liner. Accordingly, views 22 and 24 have the following differences. The fill step deposits insulator 42, wherein insulator 42 includes a dielectric material. In one embodiment, insulator 42 includes a high density plasma (HDP) oxide. In addition, the fill step causes preliner 38 to become indistinguishable from insulator 42, since the preliner and insulator are based upon a similar material. However, as a result of directional filling of insulator 42 in the trench being insufficient, the fill step results in changing undercut 36 and void region 40 becoming defined regions, such as, a defined vacancy, cavity, crevice, open region or the like. Densification can cause elongation of the void region 40 below the preliner 38. CMP reduces a thickness of the insulator 42 and nitride 34.

[0021] Referring now to Figure 5, the two views indicated by reference numerals 22 and 24 are similar to those shown in Figure 4, wherein the SOI semiconductor device 10 has been further processed with a nitride removal step. Accordingly, views 22 and 24 have the following difference. Nitride 34 has been removed, wherein nitride removal highlights (i.e., amplifies) the void region 36 in the pad-OX at the sidewall interface between regions 12 and 14.

[0022] Referring now to Figure 6, the two views indicated by reference numerals 22 and 24 are similar to those shown in Figure 5, wherein the SOI semiconductor device 10 has been further processed with a pad-OX removal step. Accordingly, views 22 and 24 have the following differences. Pad-OX layer 32 is removed with a suitable clean, such as an HF clean. The HF clean forms a corner recession (or divot) at the sidewall interface between regions 12 and 14, as indicated by reference numeral 44.

[0023] Referring now to Figure 7, the two views indicated by reference numerals 22 and 24 are similar to those shown in Figure 6, wherein the SOI semiconductor device 10 has been further processed with subsequent oxide strips. Accordingly, views 22 and 24 have the following differences. The subsequent oxide strips etch insulator 42, beginning at divot 44 and continuing down to underlying void 40, thereby forming a moat at the sidewall interface between regions 12 and 14, as indicated by reference numeral 46.

[0024] Referring now to Figure 8, the two views indicated by reference numerals 22 and 24 are similar to those shown in Figure 7, wherein the SOI semiconductor device 10 has been further processed with a subsequent gate oxide and polysilicon steps. Accordingly, views 22 and 24 have the following differences. The gate oxide step forms gate oxide 48. The polysilicon step forms a blanket polysilicon layer 50, over previously defined STI Active regions. During the polysilicon step, polysilicon deposits within the moat 46.

[0025] Referring now to Figure 9, the two views indicated by reference numerals 22 and 24 are similar to those shown in Figure 8, wherein the SOI semiconductor device 10 has been further processed with a subsequent gate patterning step where defined on an STI active region (view 24 of Figure 1), and where not-defined, the polysilicon and gate oxide are removed (view 22 of Figure 1). Accordingly, views 22 and 24 of Figure 9 have the following differences. In view 22 of Figure 9, polysilicon 50 and gate oxide 48 are removed, with the exception that some residual polysilicon remains within moat 46. In view 24 of Figure 9, the gate polysilicon includes polysilicon within moat 46, wherein the moat 46 of view 24 is the same moat 46 as referenced in view 22. This causes a hard bit failure, corresponding to a permanent breakdown of a bit in an array of the SOI semiconductor device 10.

[0026] Figure 10 is a top-down view of a portion of an SOI semiconductor device 110, having areas not susceptible to field recessions, which have been referred to herein as "moats." An active region of device 110 is generally designated by the reference numeral 112. An isolation region of device 110 is generally designated by the reference numeral 114. Semiconductor device 110 further includes transistor word lines, generally designated by reference numerals 116 and 118. An interface between an active region 112 and an isolation region 114 is generally designated by reference numeral 120. While the following discussion is particular to a single interface, it is equally applicable to more than one such interface of the semiconductor device 110.

[0027] Figures 11-18 include cross-sectional views of the SOI semiconductor device of Figure 10 at various steps of manufacture. Referring now to Figure 11, two views are shown indicated by reference numerals 122 and 124 that represent cross-sectional views of an SOI semiconductor wafer that has been processed up through FEOL (front end of line) trench etch. The SOI semiconductor substrate includes a silicon substrate 126, insulator layer 128, and silicon layer 130.

[0028] In one embodiment, the SOI semiconductor substrate includes a thin SOI substrate wherein layer 130 has a thickness on the order of less than 1100Å. Layers 132 and 134 represent pad oxide (pad-OX) and nitride, respectively. The pad-OX layer 132 includes a sacrificial oxide that protects the underlying silicon during processing of the active regions. Pad-OX layer 132 has a thickness on the order of less than approximately 100Å. Nitride layer 134 has a thickness that depends on the lithographic technique used to pattern the active region (i.e., the node wavelength g-line, i-line, DUV, 193nm, etc.). For example, the nitride layer 134 could include a thickness on the order of less than 1500Å.

[0029] At this point in the manufacturing process, cross-sectional views 122 and 124 are similar. Note that processing of the semiconductor wafer up through FEOL trench etch results in a slight over etch into bottom oxide layer 128, also referred to herein as BOX. The over etch is on the order of zero to 100Å. In addition, the FEOL trench etch creates a sidewall interface between the active region 112 and the isolation region 114, wherein the sidewall includes exposed area of silicon layer 130, pad-OX 132, and nitride layer 134. The sidewall will further include an exposed area of the BOX 128 resulting from the overetch, the exposed area having a depth approximately on the order of zero to 50Å. Accordingly, the potential for creation of an undercut (or void) at the bottom of the trench in the region of the overetch, in particular, at the silicon and BOX interface, is minimized.

[0030] Referring now to Figure 12, the two views indicated by reference numerals 122 and 124 are similar to those shown in Figure 11, wherein the SOI semiconductor device 110 has been further processed up to a pre-liner, post FEOL trench etch. Accordingly, views 122 and 124 have the following differences. A cleaning operation is performed, however, using a diluted cleaning operation so as avoid creating an undercut at the nitride/pad-OX interface. Semiconductor device 110 is then processed with an oxide to form a substantially conformal preliner 138 on the sidewall interface between regions 112 and 114. Conformal preliner 138 has a substantially uniform thickness on the order of less than 50Å. Formation of the

conformal preliner 138 also reduces the potential for creation of a void region, vacancy, cavity, crevice, or the like, at a bottom portion of the conformal preliner 138. The absence of a void region becomes significant during further processing that occurs post pre-liner.

[0031] Referring now to Figure 13, the two views indicated by reference numerals 122 and 124 are similar to those shown in Figure 12, wherein the SOI semiconductor device 110 has been further processed with a fill step, densification and CMP (chemical mechanical polish), up to post-CMP, post pre-liner. Accordingly, views 122 and 124 have the following differences. The fill step deposits insulator 142, wherein insulator 142 includes a dielectric material. In one embodiment, insulator 142 includes a high density plasma (HDP) oxide. In addition, the fill step causes preliner 138 to become indistinguishable from insulator 142, since the preliner and insulator are based upon a similar material. As a result of directional filling of insulator 142 in the trench, the fill step results in a complete filling of the trench without creation of void regions. CMP reduces a thickness of the insulator 142 and nitride 134.

[0032] Referring now to Figure 14, the two views indicated by reference numerals 122 and 124 are similar to those shown in Figure 13, wherein the SOI semiconductor device 110 has been further processed with a nitride removal step. Accordingly, views 122 and 124 have the following difference. Nitride 134 has been removed, wherein nitride removal has minimal effects on the pad-OX at the sidewall interface between regions 112 and 114.

[0033] Referring now to Figure 15, the two views indicated by reference numerals 122 and 124 are similar to those shown in Figure 14, wherein the SOI semiconductor device 110 has been further processed with a pad-OX removal step. Accordingly, views 122 and 124 have the following differences. Pad-OX layer 132 is removed with a suitable clean, such as an HF clean. In view of an absence of a void in the pad-OX at the interface of region 112 and 114, the HF clean does not form a corner recession (or divot) at the sidewall interface between regions 112 and 114.

[0034] Referring now to Figure 16, the two views indicated by reference numerals 122 and 124 are similar to those shown in Figure 15, wherein the SOI semiconductor device 110 has been further processed with subsequent oxide strips. Accordingly, views 122 and 124 have the following differences. The subsequent oxide strips etch insulator 142 on the order of

approximately 95Å, wherein the oxide strips include non-preferential etches. Accordingly, the oxide strips do not form a moat at the sidewall interface between regions 112 and 114.

[0035] Referring now to Figure 17, the two views indicated by reference numerals 122 and 124 are similar to those shown in Figure 16, wherein the SOI semiconductor device 110 has been further processed with a subsequent gate oxide and polysilicon steps. Accordingly, views 122 and 124 have the following differences. The gate oxide step forms gate oxide 148. The polysilicon step forms a blanket polysilicon layer 150, over previously defined STI Active regions. During the polysilicon step, polysilicon is fairly planar and no moats are present to fill.

[0036] Referring now to Figure 18, the two views indicated by reference numerals 122 and 124 are similar to those shown in Figure 17, wherein the SOI semiconductor device 110 has been further processed with a subsequent gate patterning step where defined on an STI active region (view 124 of Figure 10), and where not-defined, the polysilicon and gate oxide are removed (view 122 of Figure 10). Accordingly, views 122 and 124 of Figure 18 have the following differences. In view 122 of Figure 18, polysilicon 150 and gate oxide 148 are removed, and no polysilicon remains that would cause a short as in the prior integration of Figures 1-9. In view 124 of Figure 18, the gate polysilicon is free of any active regions with moats as in the prior integration of Figures 1-9. Accordingly, hard bit failures are advantageously avoided in an array of the SOI semiconductor device 10.

[0037] In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention. The various embodiments disclosed herein make use of semiconductor processing techniques known in the art and thus are not described in detail herein.

[0038] Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.